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Design and Implementation of Quintuple Processor Architecture Using FPGA

P.Annapurna[1], B.Naga Nancharamma[2]
[1]M. TECH STUDENT (VLSI), VKR, VNB&AGK COLLEGE OF ENGINEERING, GUDIVADA, JNTUK (A. P.), INDIA.
[2]M. TECH, ASST.PROF, VKR, VNB&AGK COLLEGE OF ENGINEERING, GUDIVADA, JNTUK (A. P.), INDIA.

ABSTRACT
The advanced quintuple processor core is a design philosophy that has become a mainstream in Scientific and engineering applications. Increasing performance and gate capacity of recent FPGA devices permit complex logic systems to be implemented on a single programmable device. The embedded multiprocessors face a new problem with thread synchronization. It is caused by the distributed memory, when thread synchronization is violated the processors can access the same value at the same time. Basically the processor performance can be increased by adopting clock scaling technique and micro architectural Enhancements. Therefore, Designed a new Architecture called Advanced Concurrent Computing. This is implemented on the FPGA chip using VHDL. The advanced Concurrent Computing architecture performs a simultaneous use of both parallel and distributed computing. The full architecture of quintuple processor core designed for realistic to perform arithmetic, logical, shifting and bit manipulation operations. The proposed advanced quintuple processor core contains Homogeneous RISC processors, added with pipelined processing units, multi bus organization and I/O ports along with the other functional elements required to implement embedded SOC solutions. The designed quintuple performance issues like area, speed and power dissipation and propagation delay are analyzed at 90nm process technology using Xilinx tool.
Keywords **–** FPGA, VHDL, RISC.

I. INTRODUCTION

In recent years, the processor speed is enormously increases due to the advanced computer programming language and components size. The component size can be drastically reduces due to the advanced VLSI technology. In this paper presents, five individual RISC processors are cascaded together and externally connect the local memory blocks for eliminating the thread synchronization problem. The aim of this project is to design and synthesis of Quintuple processor core for advanced concurrent computing in VHDL. Simulation refers to applying stimulus and it is a set of input parameters to the soft code and checking the validity of the output. Synthesis is the conversion of high level description of design to gate level net lists.

In the quintuple processor environment multi double the number of processors per chip with each new technology generation. In the past, processor performance was closely tied to clock frequency, which resulted in more power consumption and more successful computing performance gains. This unsustainable trend was reversed by quintuple processor core Technology that delivers processors with higher overall performance and better performance per watt. The microprocessor industry is now at a crossroads due to hitting the limit of the power that a single integrated circuit can dissipate. To continue the pattern of increasing performance, semiconductor companies have been forced to replace the single large power-inefficient processor with several smaller power efficient processors operating in parallel and at the same time, because of the growing needs rapidly increasing the design costs and the value in providing flexible platforms, many segments of embedded computing are moving away from ASIC designs to families of programmable platforms. On-chip multi processors appear to be the most promising approach to deliver competitive high performance on these programmable platforms like FPGA. As a result, both general-Purpose computing and advanced computing are being served by on-chip multiprocessor systems. The term quintuple processor core was coined to describe a microprocessor with multiple processors or cores on a single chip.

Quintuple core consists of multi connected processors that are capable of communicating. This can be done on a single chip where the processors are connected typically by a multi organization bus. Most modern supercomputers have used this multiprocessor technique. A parallel system is presented with more than one task, known as threads.

Multiprocessors are necessary to be able to communicate with each other usually via a shared memory, where values that other processors can use and stored. This introduces the new problem of thread synchronization. When thread synchronization is violated, multi processors access the same value at the same time. For this each processor to have some local memory, where the processor does not have to think about thread synchronization to speed up the processor. So that the each processor needs to have a local memory. This can be implemented by quintuple-core processor with multi cores can carry out the multi-threading more efficiently. The multi-threads are basically programmed instructions in a specific sequence to be executed with the single processor core. On the quintuple-core processor, every core presents the capability of executing a sequence of programmed instructions and thus collectively they execute the threads simultaneously. The core difference lies in the architecture, which determines the ability of the processing cores to handle the sequence of instructions simultaneously. So even if you buy a Smartphone with a multi-core processor for Rs 15,000, it will not provide the smoothness and power of high-end smart phones with multi-core mobile processors. Now, it is not only about processing muscle. For now, features such as built-in modems act as radio chips for cellular networks. Those results in slimmer and lighter smart phones. The new technology innovations in the embedded systems led to the rapid miniaturization of the electronic devices which created the necessity for Computer Aided Design tools (CAD) in the hardware design process. The newest addition to this design methodology is the hardware description language (HDL). The HDLs led to the development of new digital system CAD tools, which are now being utilized by VLSI designers. Consider the following code representation: A=A+1, When two processors P1 and P2 execute this code, a number of different outcome may arise due to the real fact that the code will be split into three parts. L1: get A; L2: add 1 to A; L3: store A.

It could be that P1 will first execute L1, L2 and L3 and afterward P2 will execute L1, L2 and L3. It could also be that P1 will first execute L1 followed by P2 executing L1 and L2, giving another result. Therefore, some methods for restricting access to shared and distributed resources are necessary. These methods are known as Thread safety or synchronization. Moreover, it is necessary for each processor to have some internal memory, where the processor does not have to think about thread safety to speed up the processor. As an example, each processor needs to have a private stack. The benefits of having a quintuple processor are as follows:

1. Less time to execute entire operation.
2. A more responsive system is created.
3. Different processors can be utilized for different tasks.
4. Faster calculations are made possible.

II. QUINTUPLE CORE ARCHITECTURE DESIGN

In this processor mainly follows the concept of parallel computing and distributed computing is applied to construct advanced concurrent computing Architecture. For this Quintuple Processor Core mainly consists of SIMD array, mapping, and local memories of designed architecture as shown in the below fig.

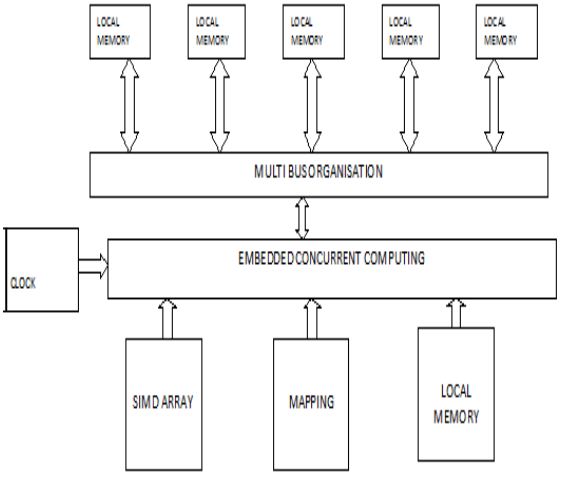

Fig.: Designed QUINTUPLE CORE Architecture

The Clock is the heart beat of any processor. The processor executes one instruction within one clock period. The Quintuple core is responsible for many concurrent computing operations and it consists of three main modules. These are Quintuple RISC Processors, I/O Ports. Generic RISC Processor are called scalar RISC Processor because they are designed to issue one instruction per cycle, similar to the base scalar processor. The concept of parallel and distributed computing Processor Core mainly consists of SIMD array, mapping, and duplicate memories.

Duplicate memories: The most important thing in quad processor mapping is the boundaries and data flow of concurrent processors. Duplicate memories are important and make a design flexible and have a high throughput for both parallel and distributed strategies and are too efficient for concurrent Architecture.

SIMD array: This SIMD array supports the multidimensional array of data. It allows the simultaneous use of multiple processors for solving a task. An SIMD array is a synchronous array of Processing Elements under the supervision of one control unit and all P.E's receive the same instruction

broadcast from the control unit, but operate on different multiple data sets from distinct data streams. It is usually loads data into its duplicate memories before starting the computation. All these are working together as a single processor that involves both the parallel and distributed concurrent strategy.

RISC Processors (RISC): In the present work, the design of an 8-bit data width Quintuple Reduced Instruction Set Computer (RISC) processor is presented. It was developed with implementation efficiency and simplicity in mind. It has a complete instruction set, program memories and data memories, general purpose registers and a simple Arithmetical Logical Unit (ALU) for basic operations. In this design, most of the instructions are uniform length and similar format. Arithmetic operations are restricted to CPU registers. The Instruction cycle consists of three stages namely fetches, decode and execute. Many numbers of RISC processors give the highest performance per unit area for parallel codes. A larger number of RISC processor cores allow a fine-grained ability to perform dynamic voltage scaling and power down. The RISC processor core with a simple architecture is easier to design and functionally verify. This processor is an economic element that is easy to shut down in the face of catastrophic defects and easier to reconfigure in the face of large parametric variation.

III. FPGA IMPLEMENTATION

Modern FPGAs are large enough to implement Quintuple-Processor Systems-on-Chip. Commercial FPGA companies also provide system design tools. To aid our design decisions, we devise a design methodology adapted to the specific challenges we are facing. Our methodology for deriving a digital logic Implementation of the required functionalities encompasses three steps, each of which comprises a set of choices. The criteria we employ to evaluate the final set of choices are complexity and scalability. We define the complexity of a unit by two metrics: the maximum operating frequency and resource usage. Lower complexity is better; that is, the unit has a higher frequency and consumes less resource. We define scalability as the ability of the unit to expand in a chosen dimension with a minimal increase in complexity.

To determine complexity and scalability, we examine the FPGA mapping of the design. In the first step, we start by choosing a particular architectural technique that provides a certain subset of the required functionalities. The second step considers the structural design choices of each architectural technique in terms of the temporal and spatial parallelism necessary to meet throughput and latency requirements. In the third step, we take into consideration the logic-implementation-specific choices driven by the constraints of the target FPGA chip. It is vital to note that the choices in all three steps are interdependent. For instance, an initially appealing architectural technique may require logic design choices that lead toward a prohibitively expensive implementation. In this case, the choice of the architectural technique has to be reexamined. In case there are feasible implementations of the selected architectural technique, the required performance can be achieved by balancing the trade-off between throughputs and operating frequency. Higher throughput necessitates higher design complexity.

IV. RESULTS

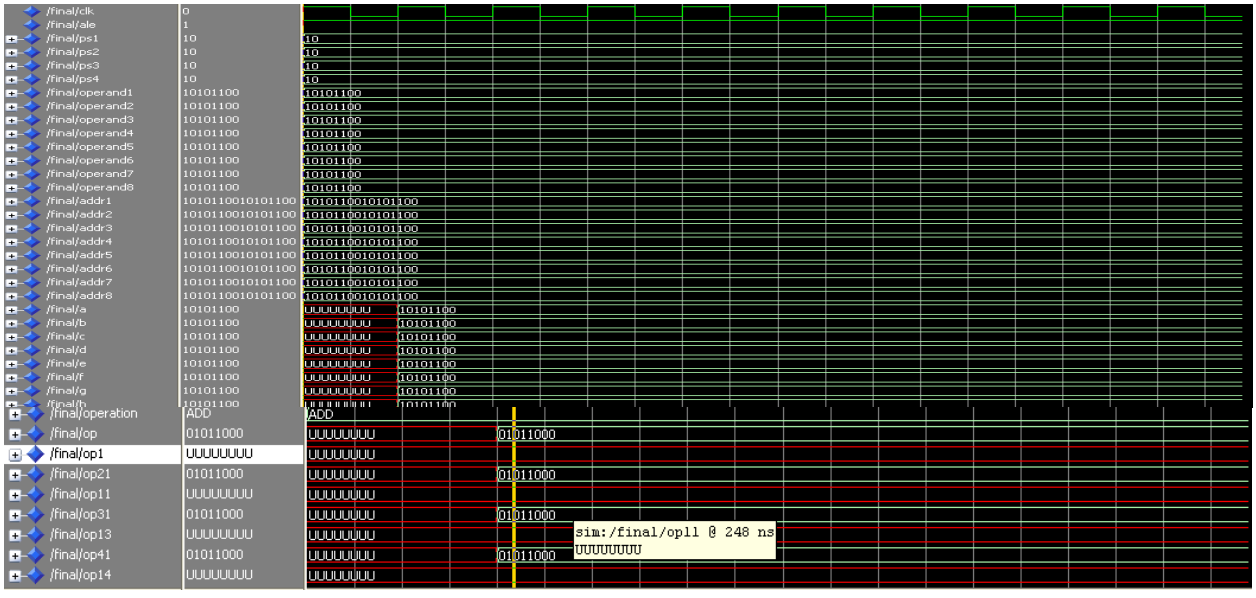

Fig.i: Single Processor Executing Addition operation in both parallel & distributing computing

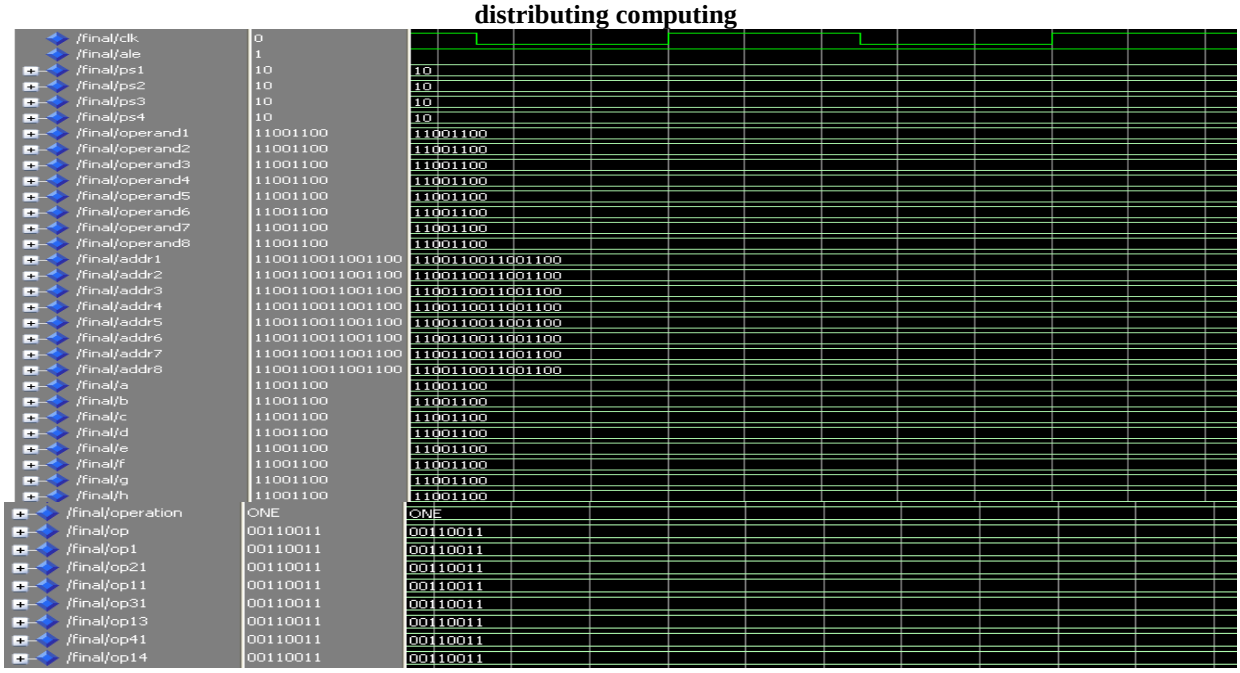

Fig.ii: Quintuple Processor Executing 1's complement Operation

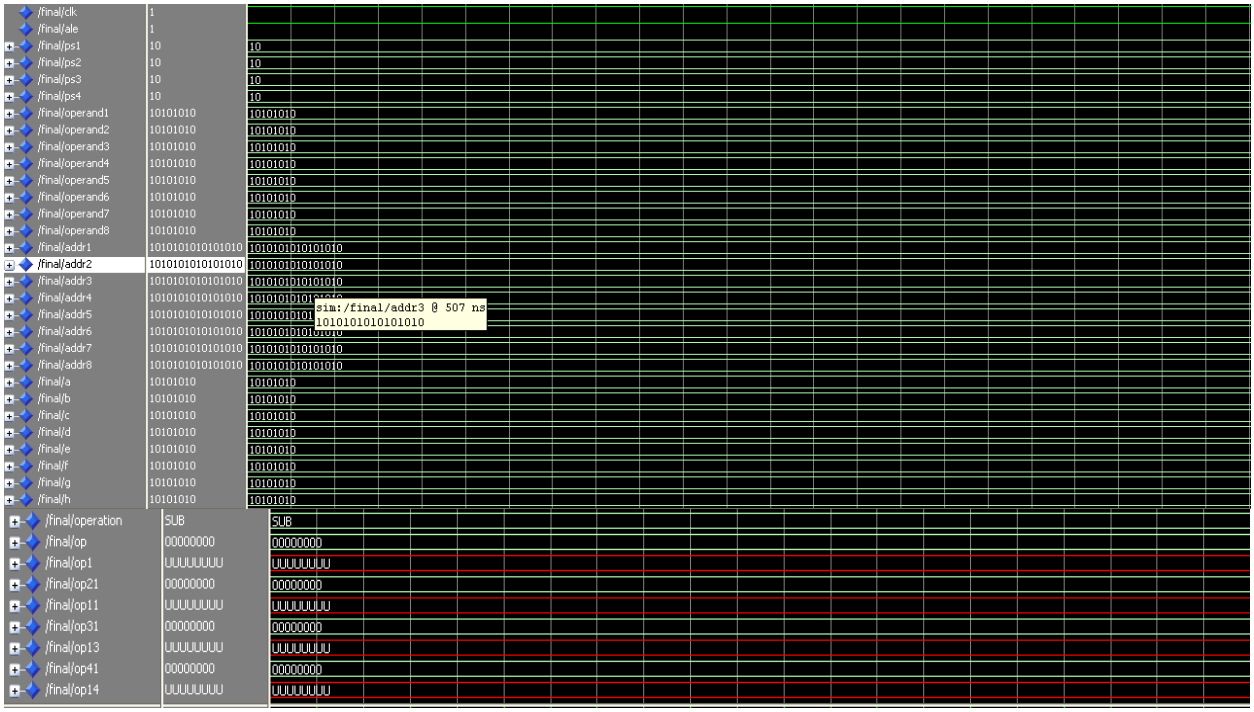

Fig.iii. Quintuple Processor Executing Subtraction operation.

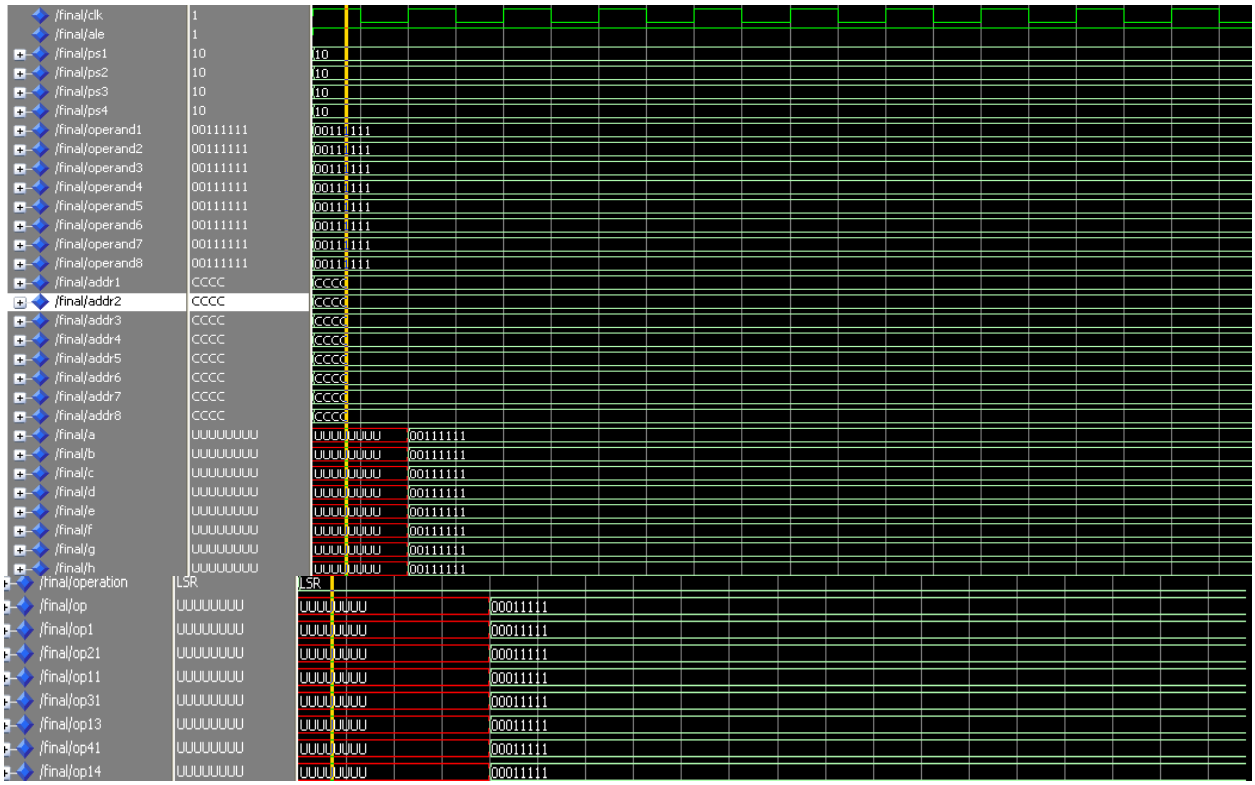

Fig.iv: Quintuple Processor Executing Logical Shift Right Operation

V. CONCLUSION

The designed quintuple processor core is very efficient and powerful core architecture, which is analyzed by using Xilinx software and simulation by using model sim simulator. Although the quintuple processor core was based on well-proven superscalar architectural techniques, including parallel execution and register renaming, these techniques were originally devised for fine-grained parallelism among instructions. The designed Quintuple core implementation using FPGA which is very advantageous to the architecture ,because it uses the parallel processing and pipielinig techniques are easily implemented in FPGA.The advanced concurrent operation of quintuple processor gives the high speed,less clock cycles to entire operation and takes less power.

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AUTHORS

P.ANNAPURNA Completed B.Tech in 2006in BITIT,HINDUPUR and presently doing her Master degree in VLSI from JNTU Kakinada University in V.K.R,V.N.B&A.G.K College of Engineering College, Gudivada. Areas of interests are VLSI,Communication systems.

B.Naga nancharamma Completed B.Tech in 2005, M.tech in 2012. Areas of interests are low power designing, real-time applications, Embedded Systems, Digital Designing. She is an Asst. Professor of ECE in V.K.R, V.N.B&A.G.K College of engineering, Gudivada.